ABSTRACT OF THE DISCLOSURE

A cache memory for performing fast speculative load operations is disclosed. The cache memory caches stack data in a LIFO manner and stores both the virtual and physical address of the cache lines stored therein. The cache compares a load instruction virtual address with the virtual address of the top cache entry substantially in parallel with translation of the virtual load address into a physical load address. If the virtual addresses match, the cache speculatively provides the requested data to the load instruction from the top entry. The cache subsequently compares the physical load address with the top cache entry physical address and if they mismatch, the cache generates an exception and the processor provides the correct data. If the virtual and physical load addresses both miss in the stack cache, the data is provided by a non-stack cache that is accessed substantially in parallel with the stack cache.